Method of manufacturing a semiconductor device and semiconductor device obtained by means of said method

The invention relates to a method of manufacturing a semiconductor device comprising a substrate and a semiconductor body in which at least one semiconductor element is formed, wherein, in the semiconductor body, a semiconductor island is formed by forming, in the surface of the semiconductor body, a first recess the walls of which are covered with a dielectric layer, after which a lateral part of the semiconductor body is removed by means of underetching via the bottom of the first recess, thereby forming a cavity in the semiconductor body above which the semiconductor island is formed, and wherein a second recess is formed in the surface of the semiconductor body, the walls of said second recess being covered with a further dielectric layer, and one of the walls of the second recess covered with the further dielectric layer being used to form a side wall of the semiconductor island.

Such a method can particularly suitably be used, inter alia, for the manufacture of, for example, semiconductor devices comprising integrated power devices. The part of the semiconductor body situated within the semiconductor island may then comprise, for example, a MOS (= Metal Oxide Semiconductor) transistor, while a part of the semiconductor body situated outside the semiconductor island may comprise one or more bipolar transistors.

A method of the type mentioned in the opening paragraph is known from European patent specification EP 1 043 769, published on 11 October 2000 under said number. In said document a description is given of the way in which in a silicon semiconductor body comprising a silicon substrate on which an epitaxial silicon layer is present, a semiconductor island of silicon is formed by covering the walls of two recesses, in the form of two parallel so-termed trenches formed in the semiconductor body, with an insulating layer. By means of etching and underetching from the bottom of the trenches, the silicon semiconductor island is formed between said trenches.

At the end faces of the trenches, isolation regions in the form of LOCOS (= Local Oxidation Of Silicon) regions (see for example Fig. 8) or so-termed trench isolation

regions (see for example Fig. 9) are formed in the semiconductor body. Consequently, the semiconductor island formed is bounded on these sides and supported by regions of silicon dioxide. It is described how, in the case of trench isolation regions, first these isolation trenches are formed by etching, after which the walls thereof are covered with an isolating layer and subsequently these trenches are filled with polycrystalline silicon. Next, the trenches on either side of the semiconductor island to be formed are created as described for the situation in which LOCOS isolation regions are applied.

A drawback of the known method resides in that it is comparatively time-consuming as it comprises many steps. As a result, the method is comparatively expensive but also the yield in terms of useful devices is adversely affected.

Therefore it is an object of the present invention to provide a method of the type mentioned in the opening paragraph, which is cheaper because it comprises fewer steps.

To achieve this, a method of the type mentioned in the opening paragraph is characterized in accordance with the invention in that for both the dielectric layer and the further dielectric layer use is made of the same dielectric layer, a lateral dimension of the second recess and the thickness of the dielectric layer being chosen such that the second recess is filled substantially completely by the dielectric layer, and the lateral dimensions of the first recess being chosen such that the walls and the bottom of the first recess are provided with a uniform coating by the dielectric layer.

The invention is based first of all on the recognition that for the isolation of the walls of the first and the second recess use can be made of the same isolating layer. This already leads to a simplification of the process. The invention is further based on the recognition that a suitable choice of the thickness of the dielectric layer and the width of the second recess enables the latter to be completely filled during the deposition process of the dielectric layer. This leads to a further simplification of the process. Said choices mean that, in practice, the width of the second recess is chosen so as to comprise approximately twice, or (slightly) less than twice, the thickness of the dielectric layer to be deposited. The width of the first recess is chosen to be so large that the walls and the bottom thereof are uniformly covered by the dielectric layer without the shape of this recess being adversely affected and without the recess being filled by the dielectric layer. By virtue thereof, in this first recess, the parts of the dielectric layer covering the walls can be formed by means of an anisotropic etch process in which the flat parts of the dielectric layer, such as those at the bottom of the

first recess, are removed again while the walls of the first recess remain covered with parts of the dielectric layer. The invention is finally based on the recognition that in such an anisotropic etch process the dielectric layer within the second recess is not, or at least not noticeably, attacked. A method in accordance with the invention may thus comprise comparatively few steps and lead to a high yield.

Therefore, in a preferred embodiment of a method in accordance with the invention, after the formation of the first and the second recess, the dielectric layer is applied over the entire surface of the semiconductor body, after which the flat parts of the dielectric layer are removed again by means of anisotropic etching.

Preferably, the second recess is formed as a ring-shaped groove surrounding the first recess, within which groove the semiconductor island is formed, the lateral dimension of the second recess being formed by the width of the groove. Adjacent or non-adjacent semiconductor islands may thus be readily formed in a semiconductor body.

In a favorable embodiment, before the dielectric layer is provided, further grooves are formed in the surface of the semiconductor body, which have approximately the same width as the said groove, as a result of which the semiconductor island is divided into semiconductor sub-islands. Said division may be such that the sub-islands are also electrically fully separated from each other, however, this is not necessary. An important advantage of this variant resides in that also the further grooves are completely filled during the deposition of the dielectric layer. These grooves thus constitute filled ribs which strengthen, as it were, the semiconductor island once the cavity has been formed, subjacent to the semiconductor island, in the semiconductor body. By virtue thereof, the risk of (mechanical) damage to the semiconductor island at that stage is reduced.

Preferably, the shape of the groove, viewed in projection, is square, and the further grooves are formed so as to extend from the middle of the sides of the square to the first recess situated in the center. An array or matrix of semiconductor islands can thus be readily formed in the semiconductor body.

In an attractive variant of a method in accordance with the invention, the semiconductor body is formed by a semiconductor substrate on which two semiconductor layers of a different semiconductor material are provided. By virtue thereof, it becomes possible, during the formation of the cavity in the semiconductor body, to remove the part of said semiconductor body that is situated below the first semiconductor layer by means of an etchant that is selective with respect to the material of the first semiconductor layer. The first semiconductor layer can be selectively removed with respect to the second semiconductor

layer in a similar manner. Besides better control of the entire process, it also becomes possible to produce semiconductor bodies having a very small thickness.

The latter variant can, for example, be implemented by applying, onto a silicon substrate on which a silicon epitaxial layer may or may not be present, a first semiconductor layer of a mixed crystal of silicon and germanium, onto which a second semiconductor layer of silicon is subsequently applied. The composition and the thickness of the Si-Ge mixed crystal are chosen such that, on the one hand, the material exhibits a maximum deviation from silicon and, on the other hand, epitaxial growth of said layers without many defects is still possible.

Therefore, to form the cavity in the semiconductor body use is preferably made, in this variant, of an etchant for silicon that is selective with respect to the semiconductor material of the first semiconductor layer, in this case the silicon-germanium mixed crystal. In a variant, after the formation of the cavity, the first semiconductor layer is removed by means of an etchant which is selective with respect to the semiconductor material of the second semiconductor layer. Preferably, the selective etching of silicon is ceased as soon as the first semiconductor layer is reached and hence borders on the cavity, after which the first semiconductor layer is selectively removed.

By virtue of the fact that a lateral dimension of the cavity is chosen to be so large that the cavity extends in the semiconductor body in said lateral direction to beyond the second recess, it is achieved that the semiconductor island is completely (electrically) insulated from the surrounding part of the semiconductor body. In the last-mentioned variant in the previous paragraph, the lateral expansion of the cavity can be limited to as far as the second recess in a simple manner, also in the case of a rectangular geometry. The etching of the first semiconductor layer is continued until the cavity has everywhere reached the second recess, at which point etching stops automatically.

In a favorable variant, use is made in the cavity-forming process of a so-termed etch-stop layer which is positioned in the semiconductor body at the lower side of the cavity to be formed. In the case of a silicon semiconductor body, use can alternatively be made for this purpose of a layer containing a mixed crystal of silicon and germanium.

Preferably, after the formation of the cavity or cavities, the walls thereof are covered with a further dielectric layer. This layer may be formed by deposition or thermal oxidation. The cavity is preferably filled with a preferably high-ohmic material, such as polydox or SIPOS. Polycrystalline silicon can very suitably be used as a filling agent for the cavity because the coefficient of thermal expansion of that material is approximately equal to

that of monocrystalline silicon, as a result of which problems during heating and/or cooling of the semiconductor body are precluded.

The invention further comprises a semiconductor body obtained by means of a method in accordance with the invention.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiments described hereinafter.

In the drawings:

Figs. 1 through 8 are both diagrammatic and, with the exception of Fig. 2 which is a plan view, cross-sectional views, at right angles to the thickness direction, of a semiconductor device in successive stages of the manufacture by means of an embodiment of a method in accordance with the invention, and

Figs. 9 and 10 are diagrammatic, plan views of different, feasible configurations for the manufacture of a larger number of semiconductor islands by means of a method in accordance with the invention.

The Figures are not drawn to scale and some dimensions, such as dimensions in the thickness direction, are exaggerated for clarity. Corresponding regions or parts in the various Figures are indicated by means of the same hatching or the same reference numerals whenever possible.

Figs. 1 through 8 are both diagrammatic and, with the exception of Fig. 2 which is a plan view, cross-sectional views, at right angles to the thickness direction, of a semiconductor device in successive stages of the manufacture by means of an embodiment of a method in accordance with the invention. The starting element used in the formation of the device 10 (see Fig. 1) is a semiconductor body 2 comprising a substrate 1, in this case a semiconductor substrate of silicon. A first epitaxial layer 11 is provided thereon by means of epitaxy, which epitaxial layer comprises a mixed crystal of silicon and germanium, and on said epitaxial layer there is provided an epitaxial-silicon layer 12 which in turn is provided with an epitaxial mixed-crystal layer 8 of silicon and germanium. The epitaxial process is concluded by the growth of a silicon layer 9. On top of said layer a hard masking layer M of, for example, silicon dioxide is subsequently deposited. The thickness of the Si-Ge layers 11 and 8 ranges, for example, between 1 and 50 nm, while the germanium content of those

layers ranges between 10 and 30 at.%. The thickness of the silicon layers 12 and 9, in this case, is in the range of 20 to 30 nm and approximately 2 μm, respectively.

Subsequently, (see Fig. 2), the hard masking layer M is patterned by means of photolithography and etching, the hatched parts of the masking layer M, as shown in Fig. 2, not being subjected to said treatments. Next, two recesses (see Fig. 3) are formed in the semiconductor body 2 by means of etching: a central, first recess 4 which is surrounded by a second recess 5 forming a closed ring. The cross-sections of Figs. 3 through 8 are taken along the line III-III in Fig. 2. The left part of these Figures shows a part of the semiconductor body 2 that is situated around the central recess 4, and the right-hand part of these Figures shows the part of the semiconductor body 2 that is situated around the second recess 5, i.e. around the part thereof that is situated on the right-hand side in Fig. 2. The part of the second recess 5 situated to the left of the central recess 4 in Fig. 2 has been omitted from Figs. 3 through 8 for the sake of simplicity. This omitted part is identical to the right-hand part of the Figs. 3 through 8.

The second recess 5 is shaped like a groove 5 whose width dimension is smaller than the lateral dimensions of the first recess 4. In this example, further grooves 7 (see Fig. 2), in this case four, are simultaneously formed in the semiconductor body 2, which further grooves connect the second recess 5 to the first recess 4, the width of said further grooves being equal to that of the second recess 5.

Subsequently, (see Fig. 3), a dielectric layer 6, in this case of silicon dioxide, is provided over the surface of the semiconductor body 2 by means of CVD (= Chemical Vapor Deposition). The thickness of this layer 6 and the dimensions of the recesses 4, 5, 7 are chosen such that the first recess 4 is provided only with a uniform coating by the layer 6, while the groove 5 (as well as the grooves 7) are completely filled by the dielectric layer 6.

Next, (see Fig. 4), the flat parts of the dielectric layer 6 are removed again by means of an anisotropic etch process, in this case a so-termed dry/plasma etch process. As a result, the walls of the recess 4 remain covered with the dielectric layer 6, while the grooves 5 (and 7) filled with said dielectric layer remain filled.

Subsequently, (see Fig. 5), in the silicon layer 12 a cavity 20 is formed below and around the first recess 4 by means of an etch process for silicon, such as an isotropic wet-chemical etch process. In this process, the layer 11, which in this example is an Si-Ge layer, serves as an etch-stop layer, which limits the depth of the cavity 20. A suitable, selective etchant is a hot ammonia solution. This etch process is then (see Fig. 6) continued, for example, until the cavity 20 extends, viewed laterally, at least as far as the filled groove 5. An

-electrically insulated- semiconductor island 3 is thus formed within the groove 5, which semiconductor island, in this example, comprises parts of the layers 8, 9 and which is bounded by the insulating regions formed by the groove 5 and the parts of the dielectric layer 6 covering the walls of the first recess 4. The cavity 20 itself may remain filled with air, as is the case at this stage. Filling it with an inert gas such as nitrogen is also possible. It is alternatively possible to evacuate and seal the cavity 20.

The further grooves 7 divide, in this example, the island 3 into four sub-islands 3A (see Fig. 2), which, consequently, are also electrically insulated with respect to each other. The grooves 7, which are also filled with the dielectric layer 6, and which are thicker than the sum of the thicknesses of the layers 8, 9 forming the island 3 and the sub-island 3A, additionally provide the latter two with a certain sturdiness. Said sturdiness can also be achieved if the grooves 7 do not form a full connection between the two recesses 4, 5. Mutual electrical insulation of the sub-islands 3A and strengthening of the island 3 and the sub-islands are functions which can also be performed separately and hence, unlike the example, do not have to be performed simultaneously.

In this example, (see Fig. 7), etching of the cavity 20 is continued by means of an etchant which selectively etches Si-Ge with respect to silicon. A suitable selective etchant is, for example, a mixture of hydrogen fluoride, hydrogen peroxide and acetic acid in a (volume) ratio of 1:2:3. In this manner, the parts of the Si-Ge-containing layers 11, 8 bordering on the cavity 20 are removed. In this manner, an island 3/sub-islands 3A are formed, in this example, which contain exclusively silicon. Subsequently, the walls of the cavity 20 are covered with a thin dielectric layer 30 of, for example, silicon dioxide. This can be achieved by a short thermal oxidation. In this example, the layer 30 is formed by first depositing a thin polycrystalline silicon layer 30, which is subsequently converted by means of oxidation into a silicon dioxide-containing layer 30.

Next, (see Fig. 8), the cavity is filled with high-ohmic polycrystalline silicon 40. Said cavity 20 may alternatively be filled with an oxygen-containing polycrystalline silicon which is known, for example, as SIPOS or POLYDOX. The advantage of polycrystalline silicon is that the coefficient of thermal expansion thereof is approximately equal to that of monocrystalline silicon.

In an attractive variant of the inventive method of this example, etching by means of the etchant which selectively etches silicon is stopped at the stage shown in Fig. 5, i.e. after only a small lateral underetch which is sufficient, however, to allow the cavity 20 to border on the Si-Ge layer. This is immediately followed by etching of the Si-Ge layer (as

shown in Fig. 9) by means of the suitable etchant. In this manner, a deeper portion of the cavity 20 may have comparatively small lateral dimensions, while the cavity 20 as a whole can still extend as far as the groove 5 without being capable of extending over an unnecessarily large distance, i.e. to beyond the groove 5. As a result, to fill the cavity 20 less material is required in this case.

The manufacture of the device 10 is then completed by forming active semiconductor elements, such as MOS or bipolar transistors, within and/or outside the island 3/the sub-islands 3A. For this purpose, use is made of processes and process steps which are customarily used in the field of IC technology. The device 10 may of course be provided with one or more other active and/or passive elements, such as diodes, resistors, coils and capacitors. A suitable pattern of connection conductors and/or bond pads is also formed, and individual semiconductor devices 10, which may comprise a discrete or semi-discrete device 10 or even an IC, are provided by means of separation techniques such as sawing.

Figs. 9 and 10 are diagrammatic, plan views of different, feasible configurations for the manufacture of a larger number of semiconductor islands by means of a method in accordance with the invention. Fig. 9 shows a hexagonal configuration of a number of combinations of first and second recess 4, 5, 4', 5' as well as further grooves 7, 7', such as in the example given above. The dotted lines show the circumference of the cavities 20, 20' formed. This configuration is roughly equivalent to a close sphere packing and is attractive because of its high degree of efficiency of the semiconductor body 2.

Fig. 10 shows a cubic configuration of a plurality of islands 3 and sub-islands 3A, as discussed in the example given above. In this, more practical, configuration the cavities 20, 20' contact each other. Fig. 10 shows an array of three cavities 20, 20', 20".

The invention is not limited to the exemplary embodiment described above, and within the scope of the invention many variations and modifications are possible to those skilled in the art. For example, devices can be manufactured having a different geometry and/or different dimensions. It is explicitly noted that the term "island" as used herein is to be understood to include also a "peninsula". This means that, for example, the second recess may have an interruption, as a result of which the island is (electrically) connected to the part of the semiconductor body situated outside said island. If the island comprises sub-islands, it is also possible that one or more of said sub-islands are connected to the part of the semiconductor body situated outside said sub-islands. Also the further recess/grooves may be provided with one or more interruptions. The island (or peninsula) may thus be subdivided into areas having a meandering structure.

It is further noted that the first semiconductor layer, which contains Si-Ge in the example given above, can be advantageously used in semiconductor elements situated within or outside the island. If a bipolar transistor is formed, for example, outside the island (as described in the patent specification mentioned in the introductory part), the Si-Ge layer can be used there to improve properties of the bipolar transistor. Within the island, where for example MOS transistors can be formed, the (mechanical) stress associated with the presence of a Si-Ge layer may be used, for example, to influence the mobility, for example, not in an PMOST but in an NMOST.

It is to be noted that materials other than those mentioned in the examples may alternatively be used within the scope of the invention. Also other deposition techniques may be used for the above-mentioned materials or other materials, such as epitaxy, CVD (= Chemical Vapor Deposition), sputtering and vaporization. Instead of wet-chemical etching methods use can alternatively be made of "dry" techniques, such as plasma etching, and vice versa.

Finally, it is noted that the device may comprise additional active and passive semiconductor elements or electronic components, such as a larger number of diodes and/or transistors and resistors and/or capacitors, whether or not in the form of an integrated circuit. The manufacturing process is of course efficiently adapted thereto.